REMARKS

Claims 1-21 are pending in the application. Claims 1-10 are allowed, and claims 19-21 have been determined to contain allowable material. Claims 11-18 were rejected. In response to the above-identified Office Action, Applicant does not amend any claims, cancel any claims, or add any new claims. Reconsideration of the rejected claims in light of the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 11-18 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,991,520 issued to Smyers *et al.* ("*Smyers*") in view of U.S. Patent No. 4,682,284 issued to Schrofer ("*Schrofer*"). For the reasons explained below, Applicant believes that the references of record fail to teach or suggest the subject matter of the rejected claims.

As to claim 11, that claim recites a system of processing packets in a bus switch comprising several elements, including means for storing data in queues and means for directing a set of incoming data to the appropriate queueing means. These elements clearly show that the packet processing system contains more than one queue, because the word "queue" is pluralized, and because there is a means for directing a set of incoming data to the appropriate queueing means. No such directing means would be necessary if there was only one queue.

Smyers depicts and describes only a *single* queue (*see* Fig. 2, element 30, and col. 6, line 15+), which contains three buffer descriptors. (Strictly speaking, *Smyers* describes a doubly linked list of buffer descriptors.) *Smyers*'s buffer queue seems to be associated with a data stream between an application and a node on the bus structure (*see* col. 6, lines 2+), and data packets are directed to the queue based on a channel number allocated to the application-node communication stream.

Thus, *Smyers* is different from the system of claim 11 at least because it has only one queue, and because packets are directed to the queue based on a channel number, not based on a cycle number in which the set of data arrive. The secondary reference, *Schrofer*, is relied upon for elements of uncertain relevance to the claim (*e.g.* processing data within one cycle and queue validity checking, neither of which are mentioned in

claim 11). The Examiner does not indicate, and Applicant has been unable to find, a teaching or suggestion of storing data in more than one queue and directing sets of incoming data to an appropriate queueing means, within *Schrofer*.

For at least these reasons, Applicant respectfully submits that *Smyers* and *Schrofer* fail to teach or suggest the material of claim 11, and requests that the Examiner withdraw this rejection.

As to claim 12, that claim depends upon claim 11, and is patentable for at least the reasons discussed in support of that base claim. Applicant respectfully requests that the Examiner withdraw the rejection of claim 12 also.

As to claim 13, that claim recites a switch in a network comprising a number of elements, such as a buffer memory including at least three egress queues. *Smyers* discusses operations of only a single queue, so the reference is two queues short. In addition, *Smyers*'s queue accepts incoming data which is subsequently delivered to an application program. Thus, the queue is not an "egress" queue, as claim 13 requires. It seems possible that the Examiner is reading the three *data buffers* of *Smyers*'s Figs. 2 and 5 as the claimed *egress queues*. However, a data buffer is different than a queue, because a data buffer is a portion of memory to contain a data packet, while a queue is a data structure to manage one or more data buffers as a list or array.

Regarding *Schrofer*, the Examiner relies on the reference for several points that are not present in claim 13 or its dependent claims. For example, the Examiner mentions that "*Schrofer* teaches reading/writing to occur during a single cycle." However, none of claims 13-18 require reading or writing during a single cycle.

For at least the foregoing reasons, Applicant respectfully submits that *Smyers* and *Schrofer* fail to teach or suggest at least the element of a buffer memory including at least three egress queues. The Examiner is requested to withdraw the rejection of claim 13.

As to claims 14-18, those claims depend directly or indirectly upon claim 13, and are patentable for at least the reasons discussed in support of their base claim. Applicant respectfully requests that the Examiner withdraw the rejections of these claims also.

II. Allowed Claims

Applicant notes with appreciation that the Examiner has determined claims 1-10 to be allowable.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-21, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

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Respectfully submitted,
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Nadya Gordon — June 30, 2005